activates at least some of the plurality of independent clock signals in response to received condition data during an active mode.

8 (Once Amended) A power consumption reduction circuit comprising:

a memory clock source for a graphics controller; and

a memory clock divider circuit, operatively coupled to the memory clock source, that generates divided memory clock output signals as a plurality of corresponding independent clock signals to a number of memory interface circuits for differing processing engines and selectively activates at least some of the plurality of independent clock signals in response to received condition data;

an engine clock source operatively coupled to a switching circuit that generates an output engine clock signal that is selectively coupled as a clock signal to each of a plurality of registers associated with at least one of: a video overlay engine, a video capture engine, I2C control logic and a multimedia port, such that the switching circuit disables the output engine clock signal in response to receiving condition data; and

a plurality of memory read latch circuits and a memory read latch control circuit operative to dynamically activate and de-activate the plurality of memory read latches based on detected memory read requests to facilitate memory access activity based power reduction.

13. (Once Amended) A power consumption reduction method comprising:

generating divided memory clock output signals as a plurality of corresponding independent clock signals to a number of memory interface circuits for differing processing engines;

selectively activating at least some of the plurality of independent clock signals in response to received condition data;

selectively coupling an engine clock signal to each of a plurality of registers associated with at least one of: a video overlay engine, a video capture engine, I2C control logic and a

multimedia port to selectively disable the output engine clock signal in response to receiving condition data; and

dynamically activating and de-activating a plurality of memory read latches based on detected memory read requests to facilitate memory access activity based power reduction.